

# MS-7636 Ver: 1.3 uATX(244mm X 240mm)

## CPU:

INTEL - Lynnfield/ Clarkdale LGA 1156

## System Chipset:

INTEL-IBEXPEAK PCH (H - 55)

## OnBoard Chipset:

Clock Gen:ICS 4105B

IDE X1 JMB-368

HD Audio Codec:ALC889

LAN:RTL8111D 10/100/1000

SIO:F71889

Flash ROM: 64 Mb SPI (CHIP)

## Main Memory:

DDRIII (800/1066/1333MHz) \* 4 (Dual Channel)

## Expansion Slots:

PCI Express (X16) Slot \* 1

PCI Express (X1) Slot \* 2

PCI Slot \*1

## PWM:

Controller: uP6206

( 3-Phase use STD MOS -- 95W )

OV by uP6264 or SIO

uP6103 (CPU\_VTT)

Linear (PCH)

uP6103(DDR)

GPU Power -ISL6314

## ACPI: uPI+SIO

## Other:

SATA(SATA2-300MB/s) \*6

USB2.0 \*10 (Rear\*4 / Front\*6)

PRINT Header \*1

COM pin header \*2

TPM Header \*1

on BOARD BUZZER

D-SUB \*1

DVI PORT\*1

HDMI PORT\*

## BOM SKUs

H55:chiset

S:solid cap

EL:EL cap

G:giga lan 8111DL

M:Miga lan 8103EL

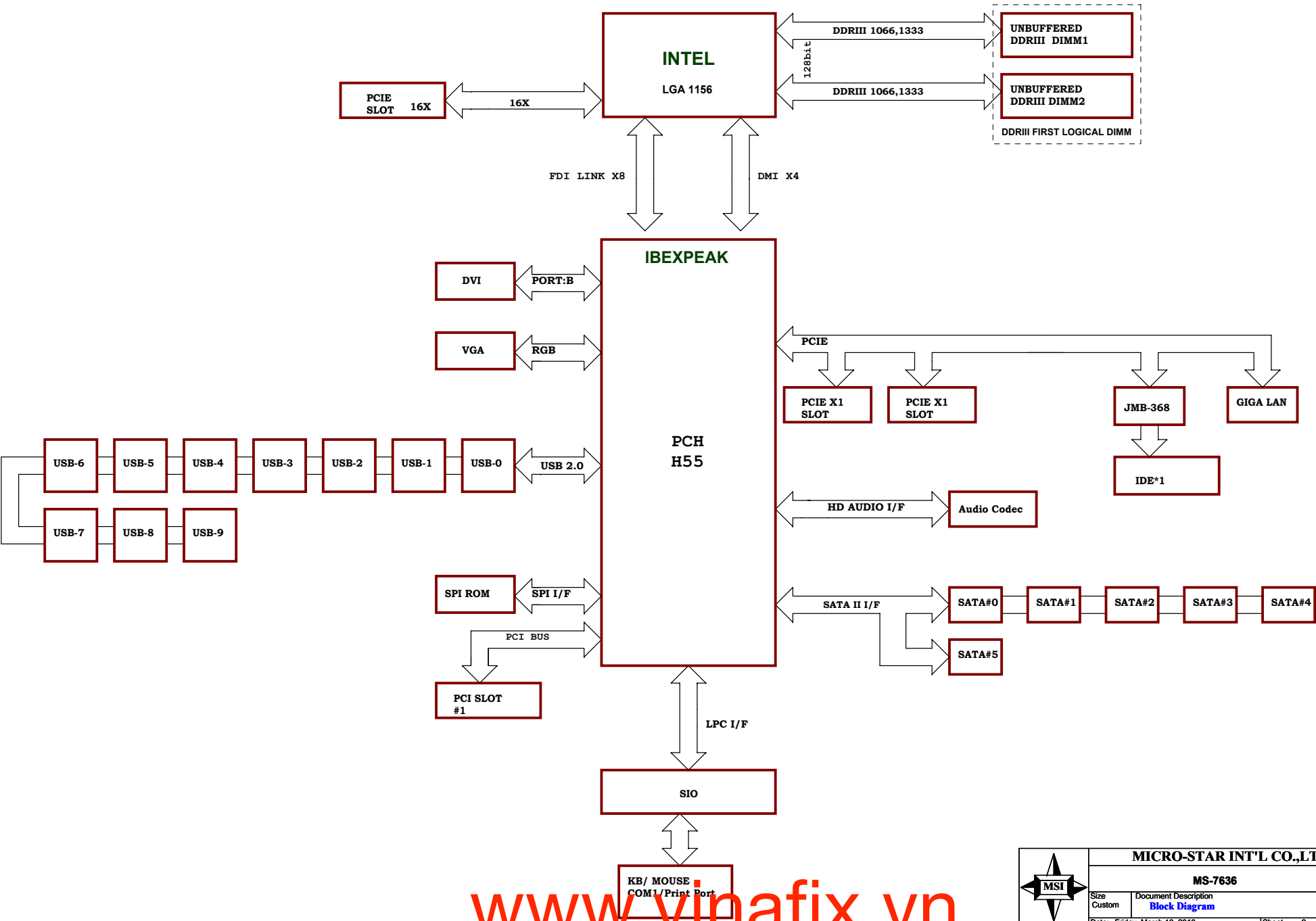
6: 6 ports

DVI: DVI Stuff

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### DDR DIMM config.

Device	Address	Clock
CHA DIMM1	10100001B	MEM MA CLK H0/L0 H1/L1
CHB DIMM2	10100000B	MEM MB CLK H0/L0 H1/L1

### PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INT#A PCI_INT#B PCI_INT#C PCI_INT#D	PCI_REQ0# PCI_GNT0#	AD16	PCH CLKOUT_PCI<0>
TPM				PCH CLKOUT_PCI<3>
SIO				PCH CLKOUT_PCI<2>

### PCI RESET DEVICE

IBEXPEAK	
Signals	Target
PCIRST#_PCH	PCISLOT1
PLTRST_BU1#	JMB368 IDE
PLTRST_BU2#	PCIE*16 / *1
PLTRST_BU3#	LAN&TPM
PLTRST#	SIO





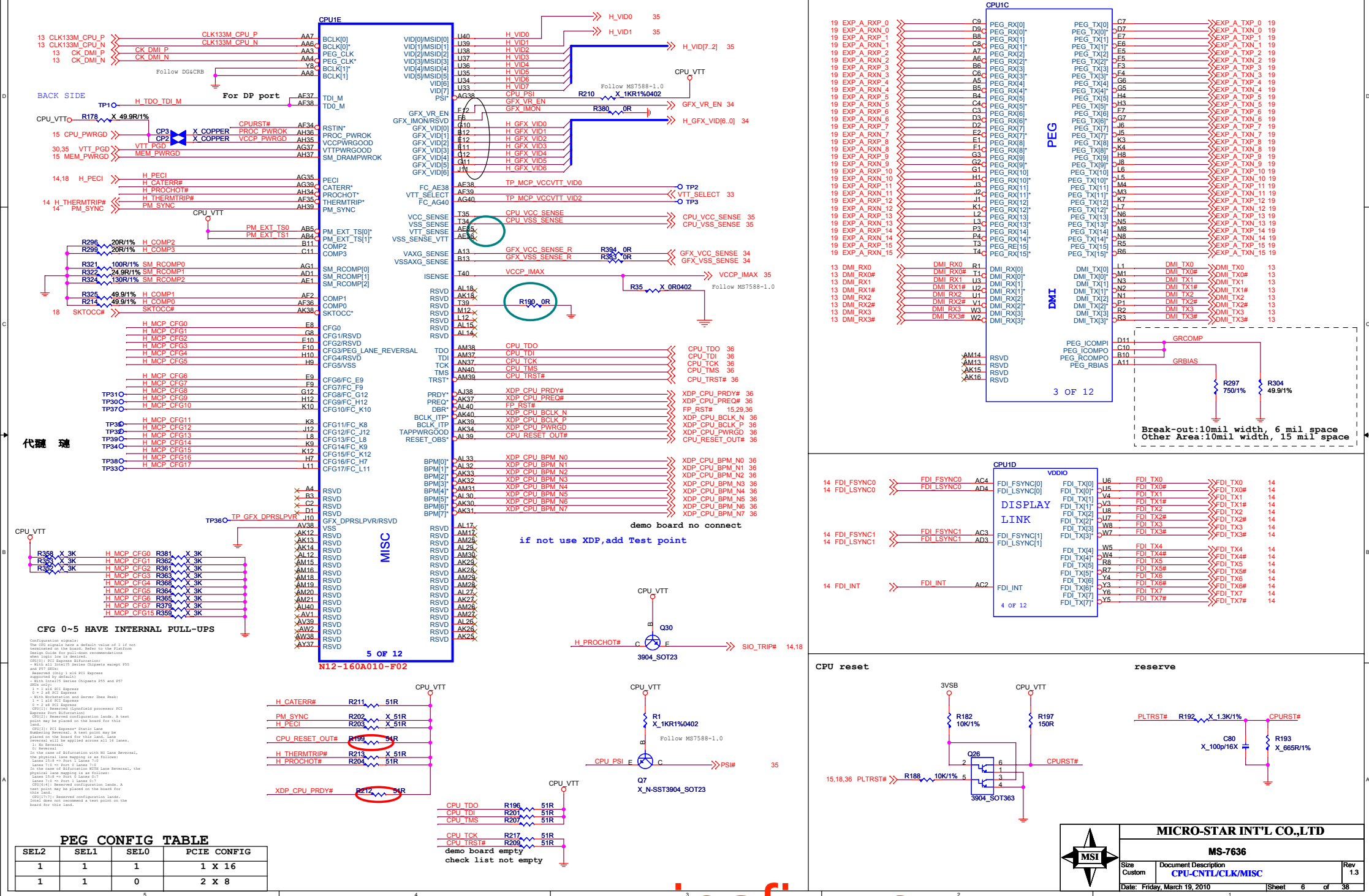
## History

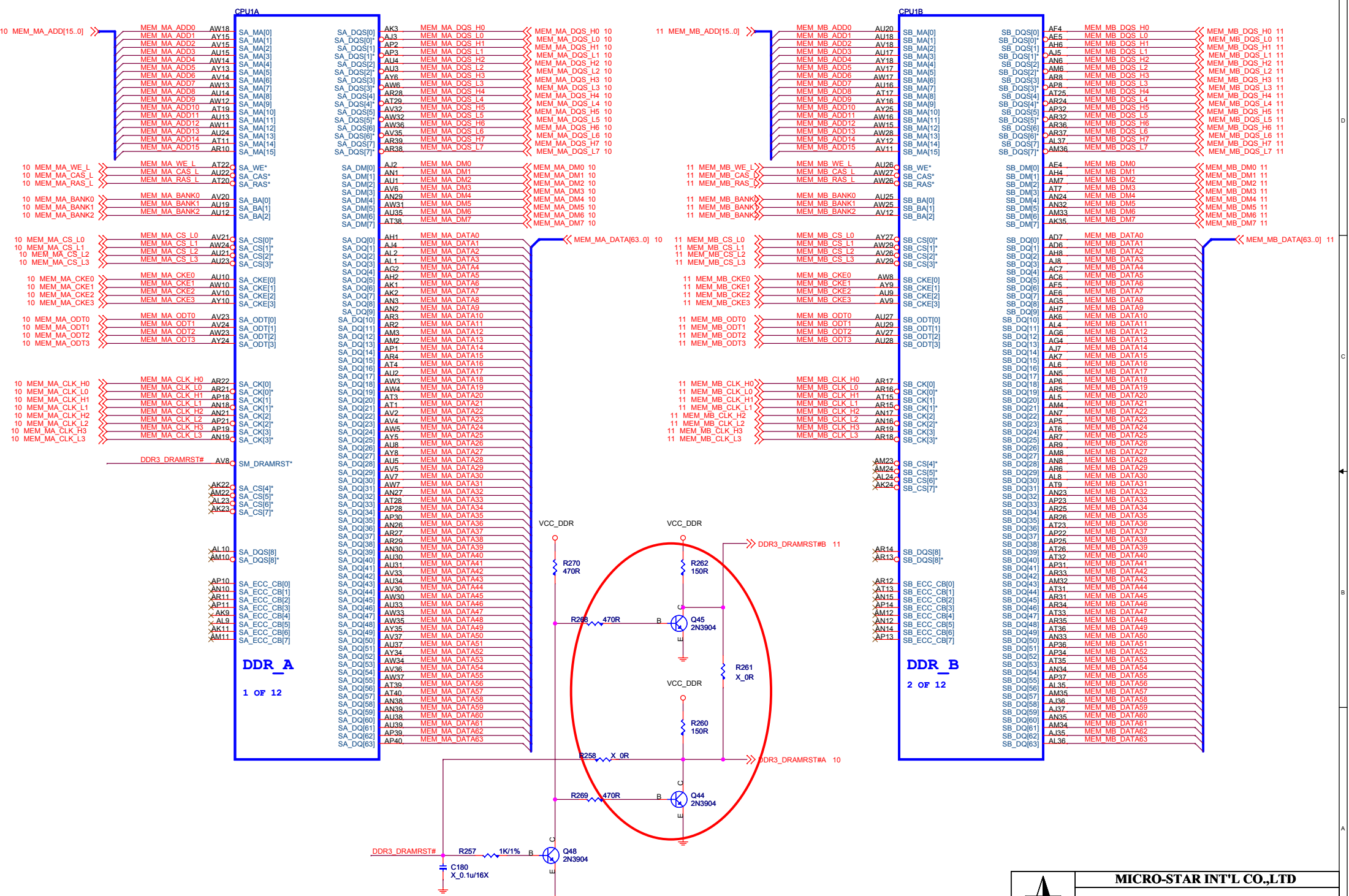
- 1.2009-10-13 Change VCC\_SENSE to CPU\_VCC\_SENSE
- 2.2009-10-13 Add HDMI circuit,change USB circuit,JSP1 circuit update
- 3.2009-10-13 update NCT3016 circuit ,add VTIN3 circuit for VRM MOS
- 4.2009-10-18 Add C589 C590
- 5.2009-10-18 Add R561 R562 For HDMI HPDET
- 6.2009-10-20 Add R602,Swap HDMI wire for layout
- 7.2009-10-21 NCT3016 circuit update:add R637 Q65 R592,Change U27 pin16 tp NCT\_GPIO16,delete C121
- 8.2009-10-21A NCT3016 citcui update:add Q85,chang SATA1&SATA2 to SATA1\_2
- 9.2009-10-23 change JUSB2 & JUSB1 for layout
- 10.2009-10-23A NCT3016 circuit update:add R850
- 11.2009-10-24 delete VCCGATE and DUALGATE circuit
- 12.2009-10-26 delete C534
- 13.2009-10-26 Swap RN40

## MS-7636-1.3

- 1.2010-02-23 Add MH7 MH8 MH9 R545

A48/Y8 ,these signals are for 120 MHz from the Intel® CPU\_P /CLKOUT\_BCLK1\_P and CLKOUT\_DP\_N and CLKOUT\_BCLK1\_N. Leave as NC on the PCH and connect directly to GND at the processor. 120MHz clock is used for embedded DisplayPort which is no supported on Desktop designs.





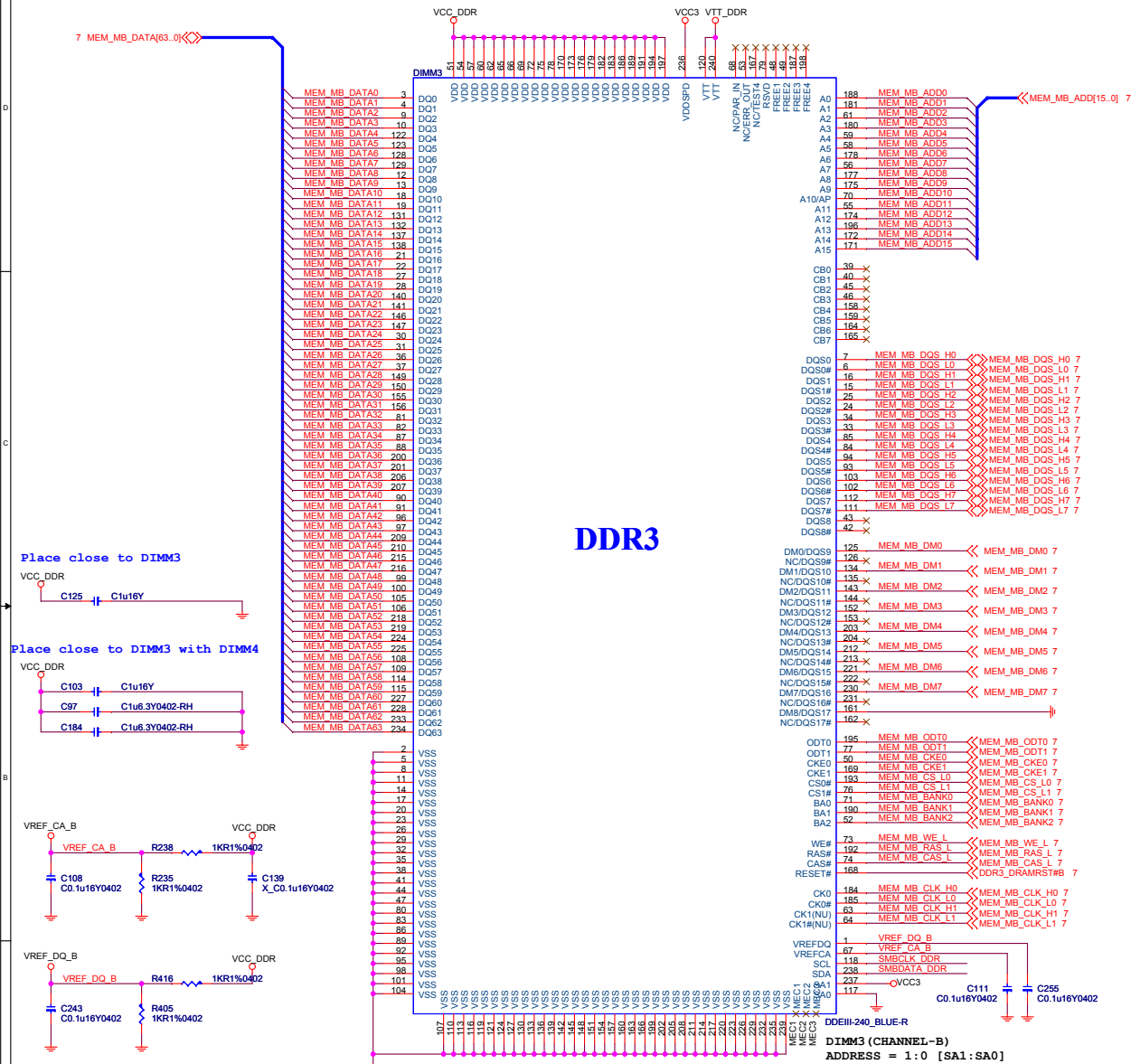


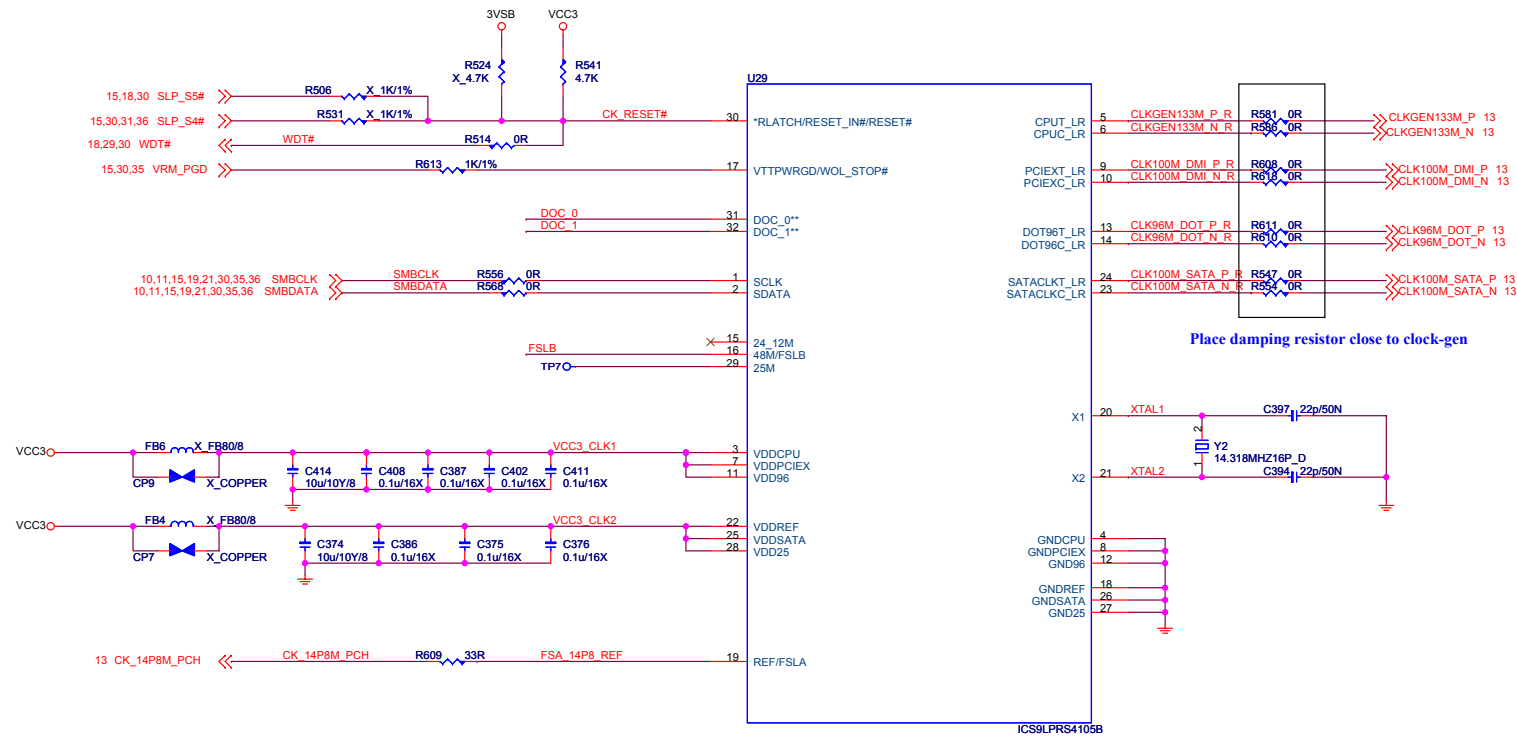




# DDR3 DIMM\_B1

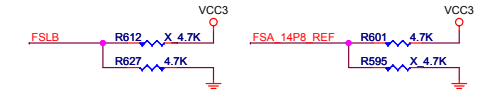
# DDR3 DIMM\_B2





## CLOCK GEN STRAPPING

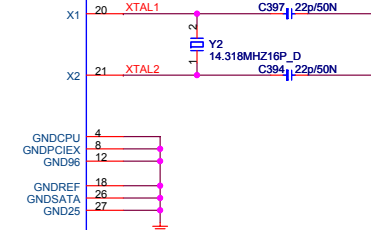
FS4	FS3	FS2	FSB	FSA	CPU	Spread
B0b4	B0b3	B0b2	B0b1	B0b0	Mhz	
0	0	0	0	0	100.00	-0.5
0	0	0	0	1	133.33	-0.5
0	0	0	1	0	200.00	-0.5
0	0	0	1	1	166.66	-0.5



Pin16: 48MHz clock output. / 3.3V tolerant input for CPU frequency selection. Low voltage threshold inputs, see input electrical characteristics for Vil\_FS and Vih\_FS values.

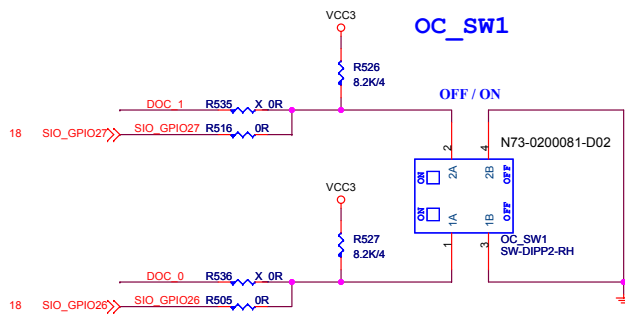
Pin19: 14.318 MHz reference clock./ 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil\_FS and Vih\_FS values.

Place damping resistor close to clock-gen



## OC

DOC\_0\*:Dynamic Over Clocking pin: real time frequency selection 0: Normal; 1: Frequency will transition to a preprogrammed value in the I2C.

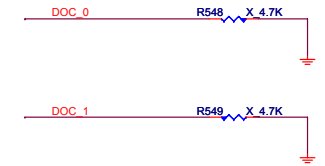
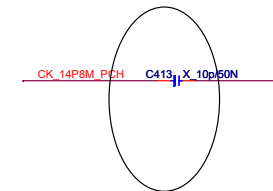


OFF=1 ; ON=0

DOC	TABLE
1 0	CPU FREQUENCY
1 1	133 MHz ( default )
1 0	142 MHz
0 1	150 MHz
0 0	166 MHz

( Default ) OFF / OFF  
OFF / ON  
ON / OFF  
ON / ON

EMI

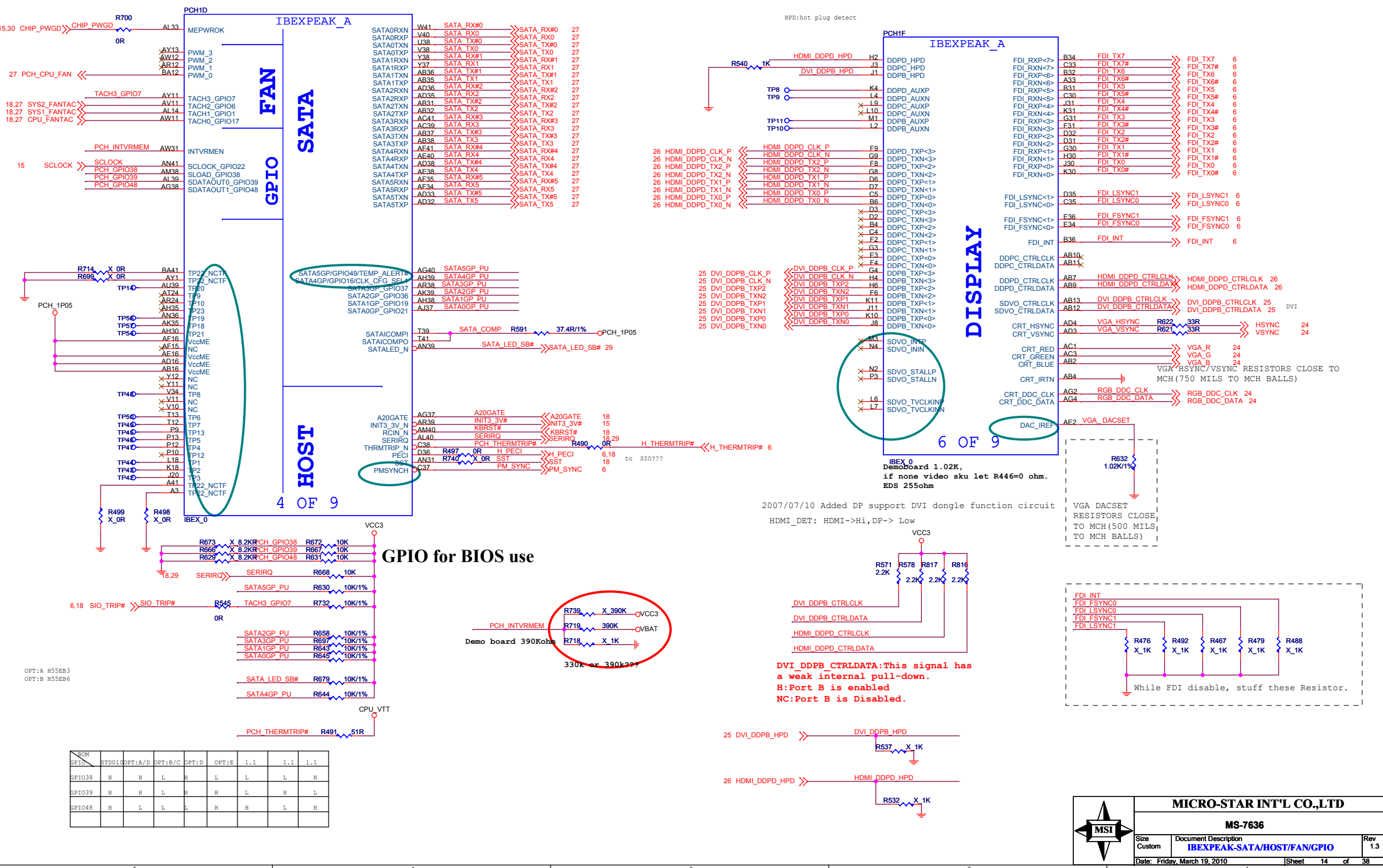


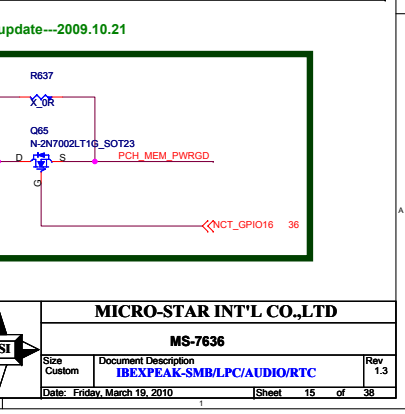
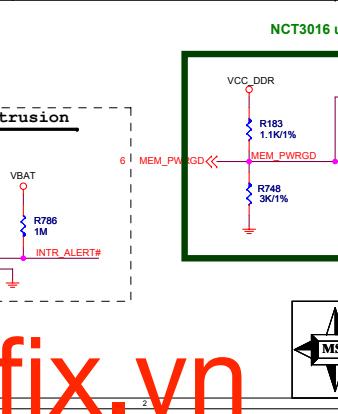
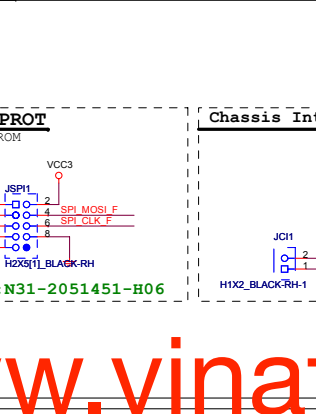
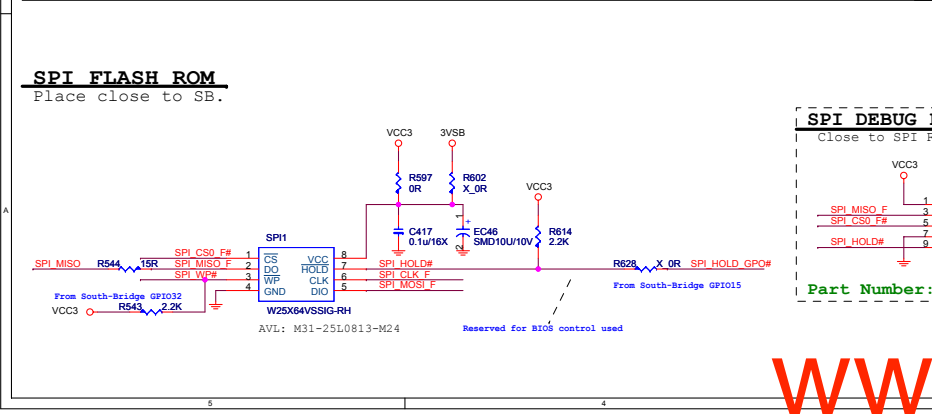
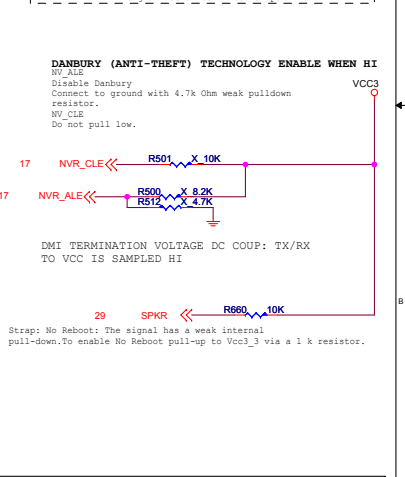
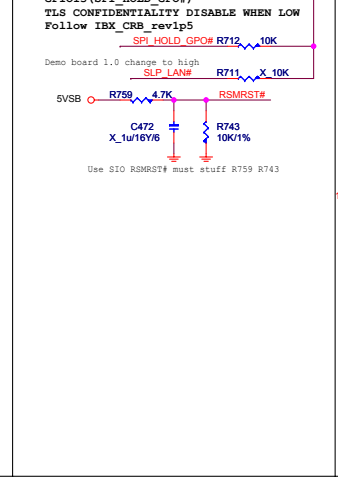
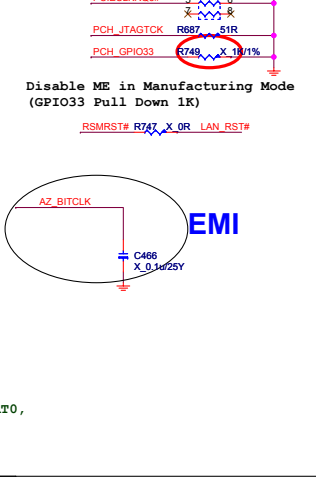
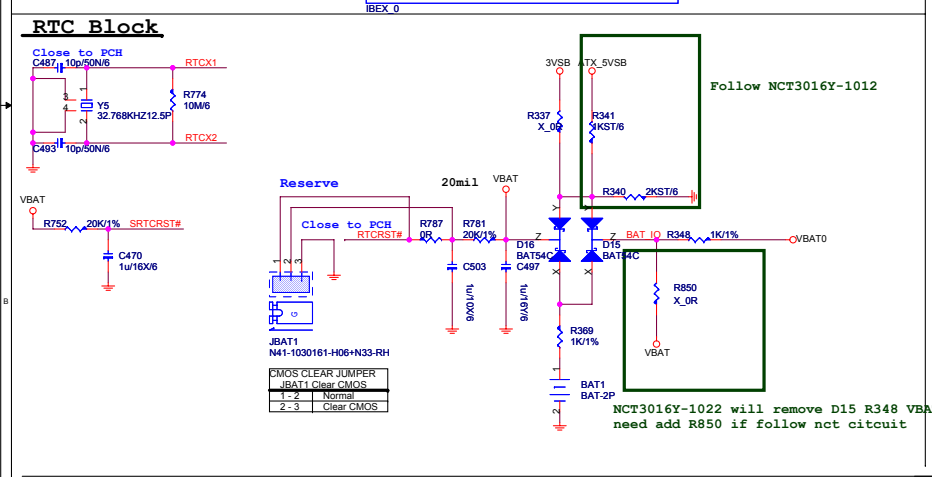
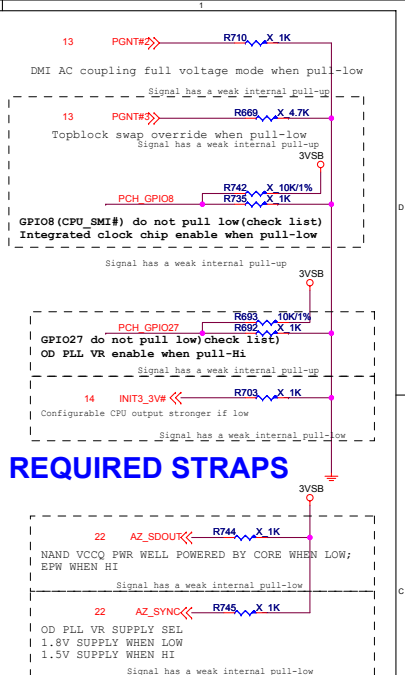
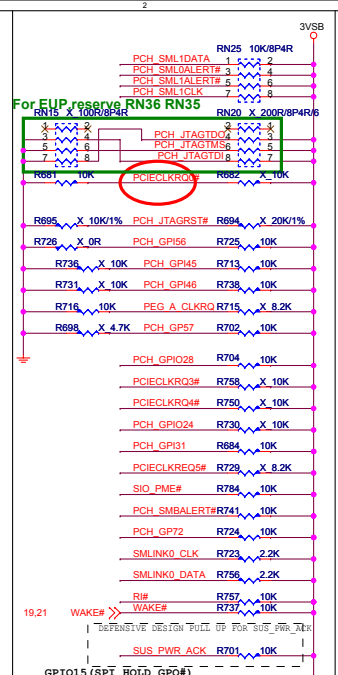
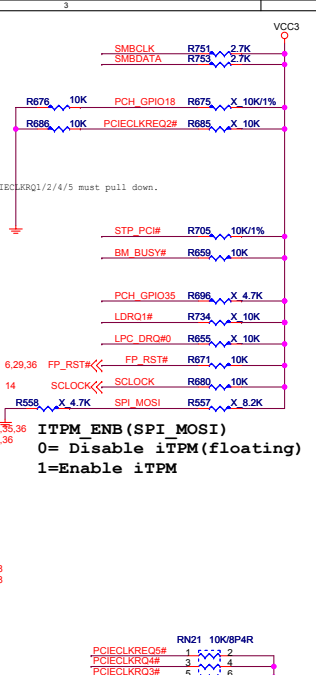
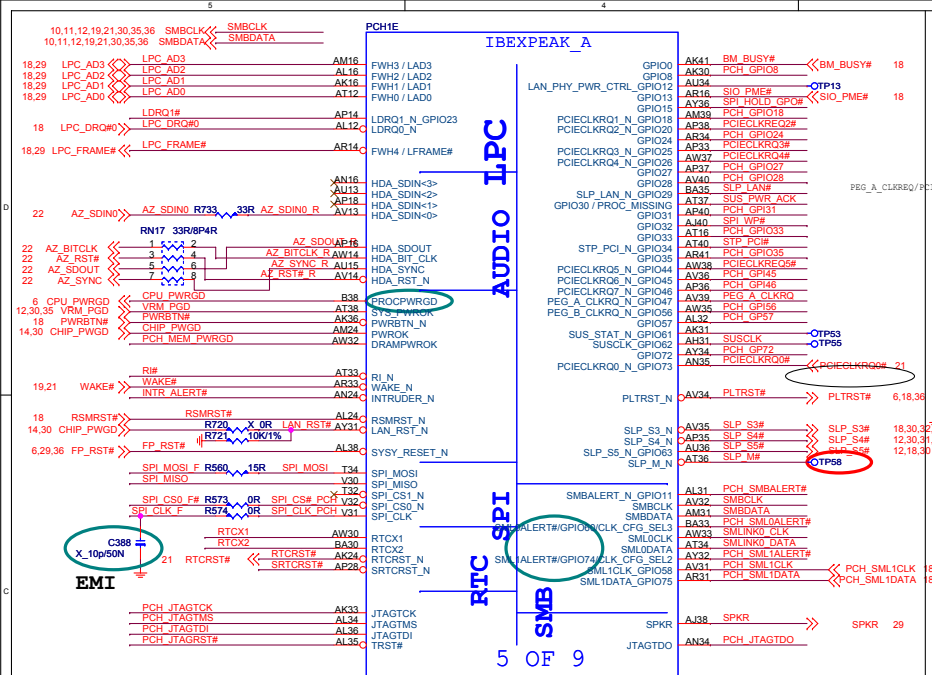
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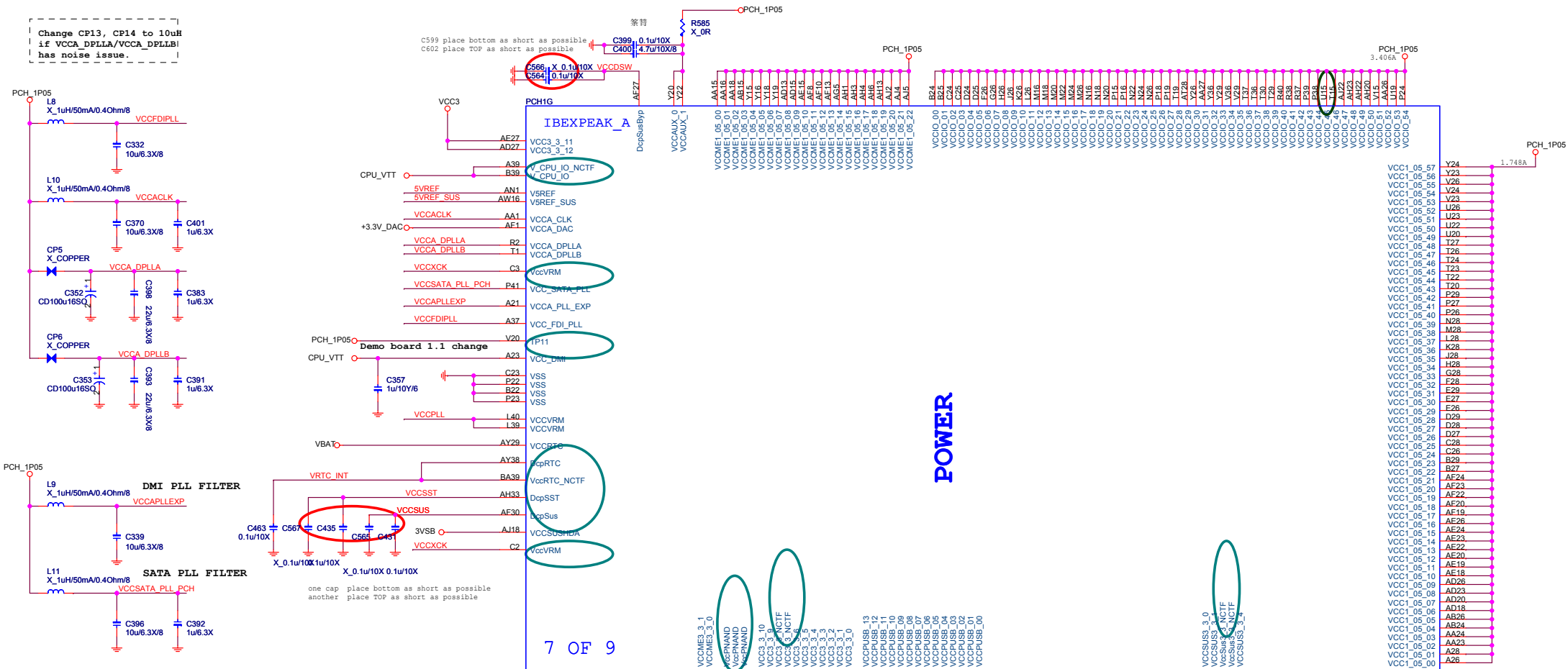






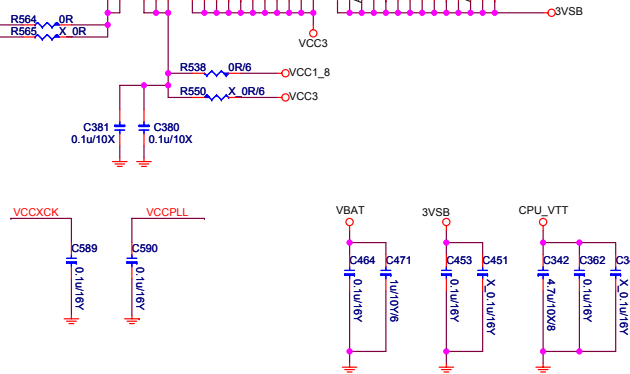
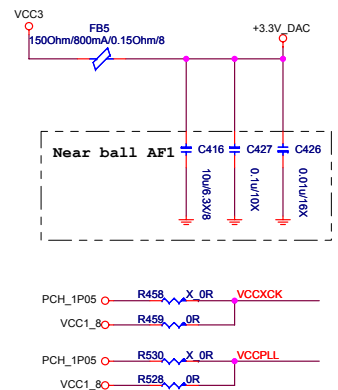
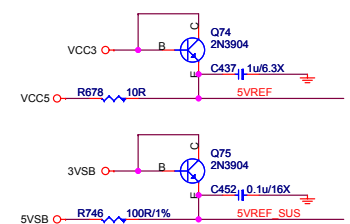
Change CP13, CP14 to 10uH  
if VCCA\_DPLLA/VCCA\_DPLLH  
has noise issue.

C599 place bottom as short as possible  
C602 place TOP as short as possible

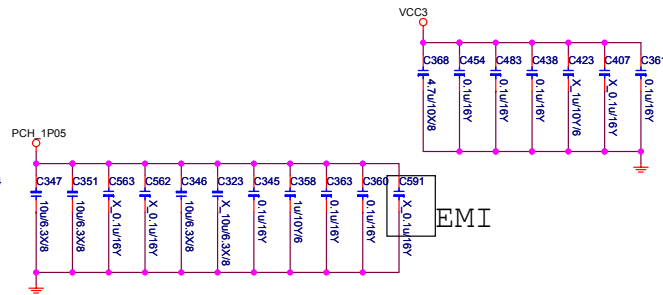


# 5VREF & 5VREF\_SUS Sequencing Circuit

V5REF must be powered up before VCC3 or after VCC3 within 0.7V.  
Also, V5REF must power down after VCC3 or before VCC3 within 0.7V.  
This rule is also applies to V5REF\_SUS and 3VSB.  
However, the 3VSB is derived from the 5VSB on the power supply  
thru a voltage regulator and therefore, they can satisfy the requirement.



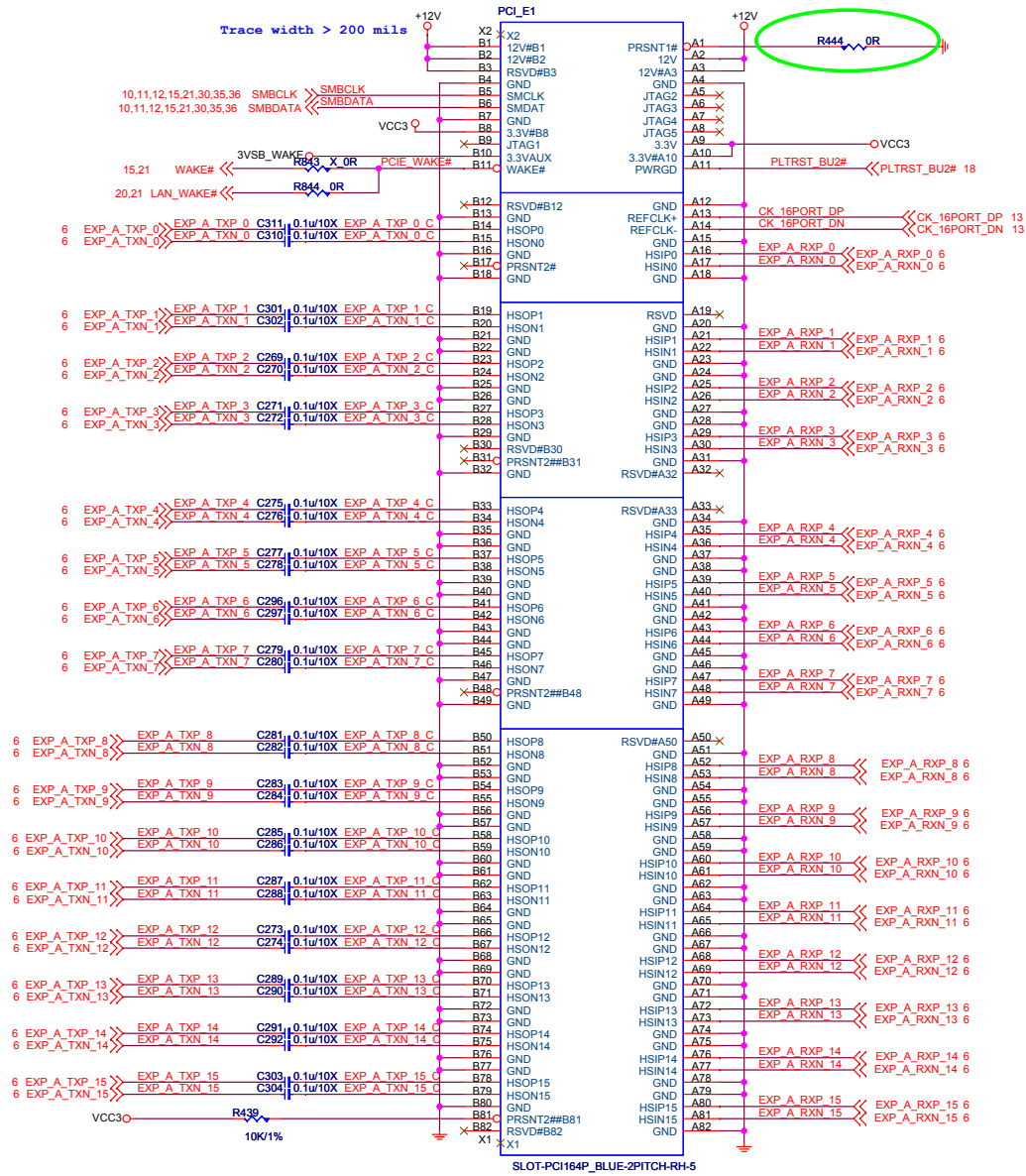
## PCH decoupling cap



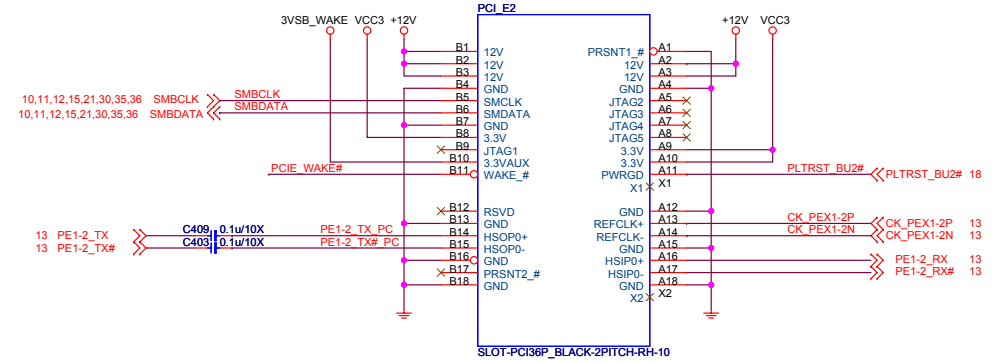




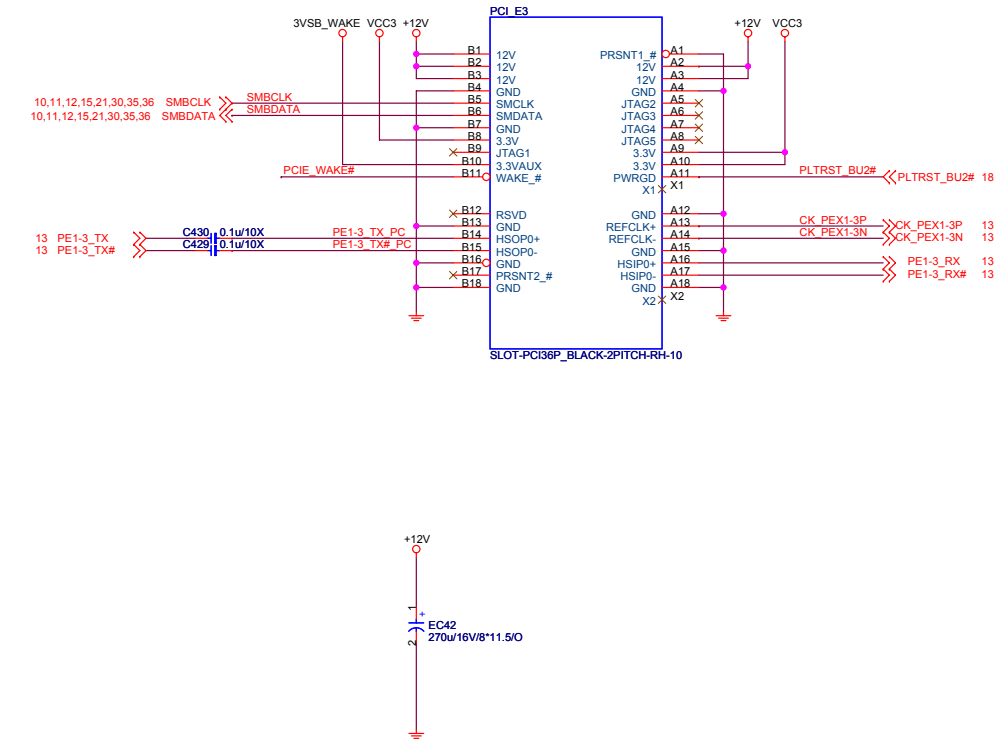
# PCI Express X16 Slot



## PCI EXPRESS x1-PORT2



## PCI EXPRESS x1-PORT3

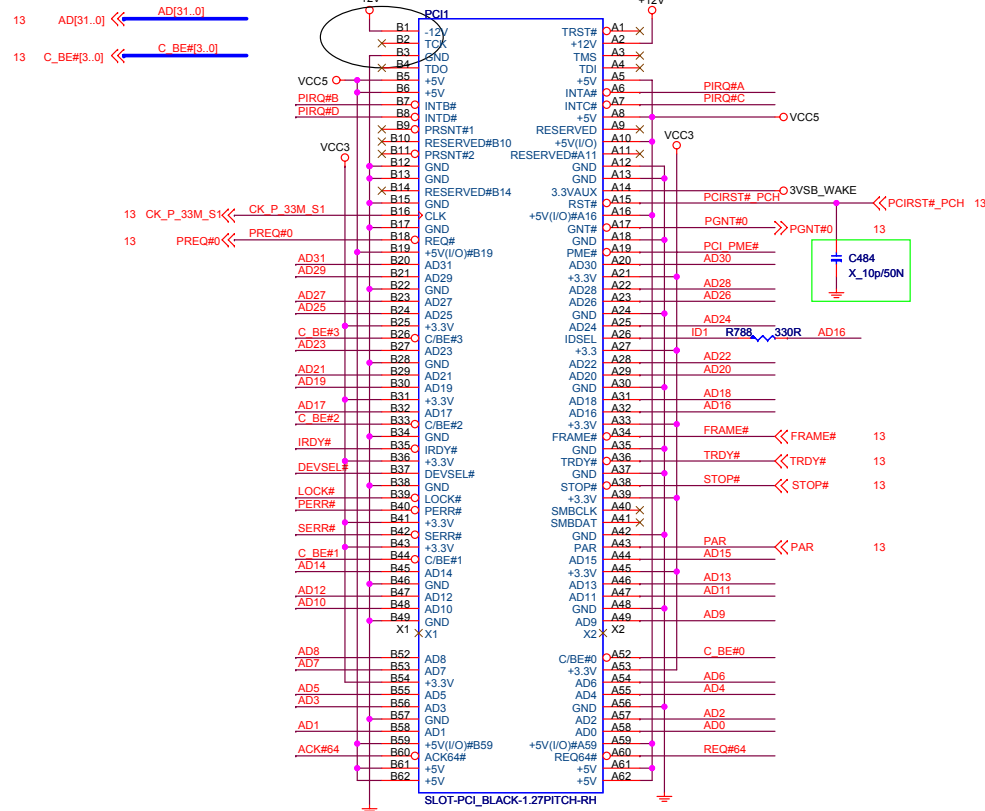


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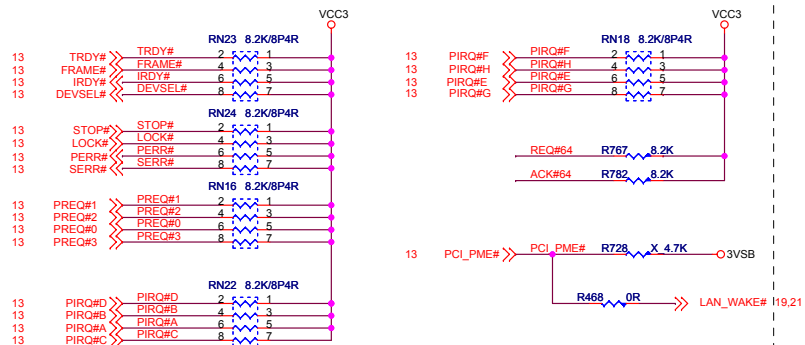
Size	Document Description	Rev
Custom	PCIe x16/x1/x1 Slots	1.3
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# PCI SLOT 1 (PCI VER: 2.2 COMPLY)

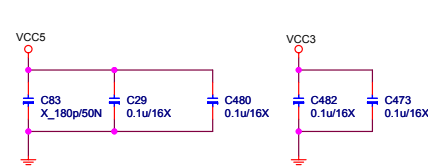


IDSEL = AD16  
MASTER = PREQ#0  
PIRQ#A

## PCI PULL-UP / DOWN RESISTORS

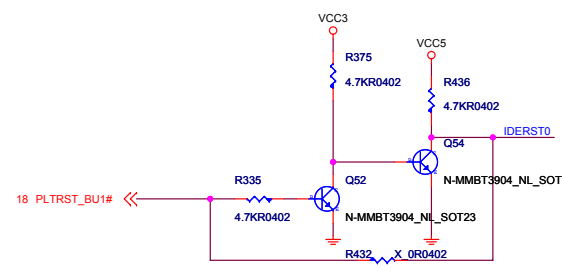
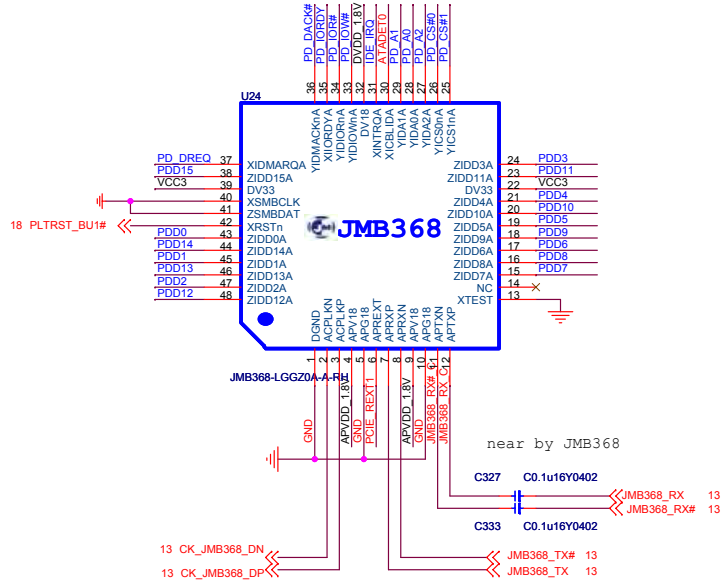
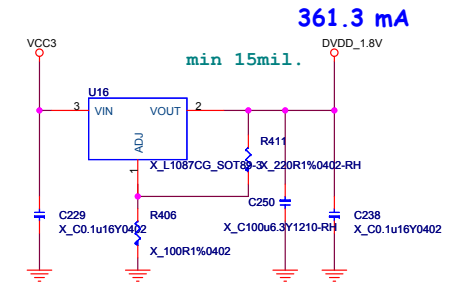
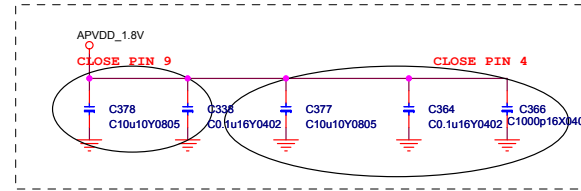
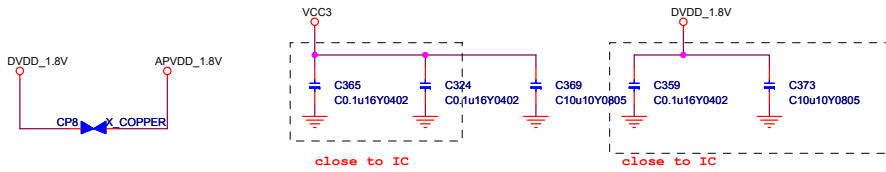


## PCI SLOT DECOUPLING CAPACITORS

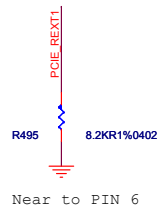
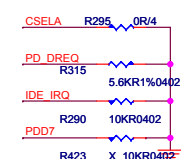
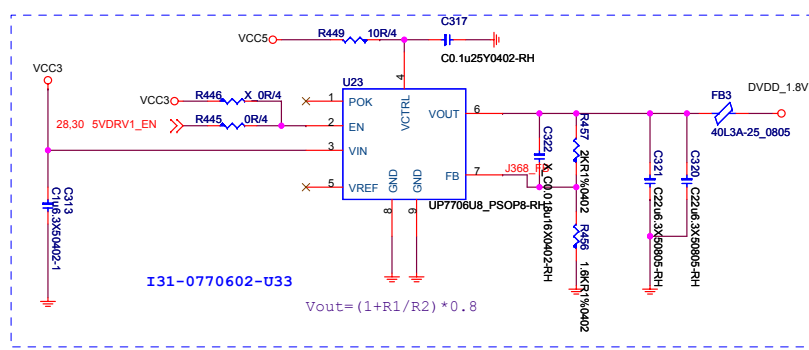
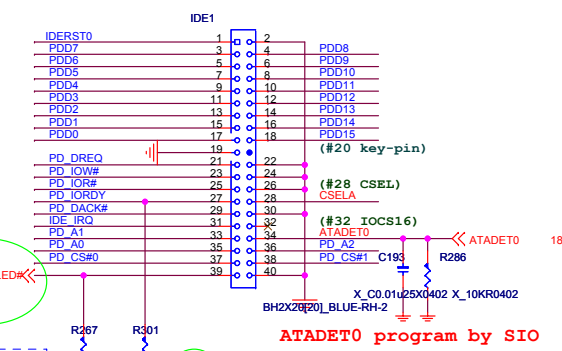








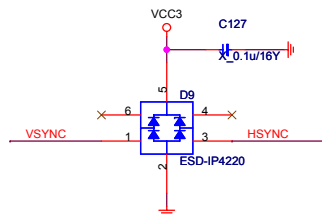
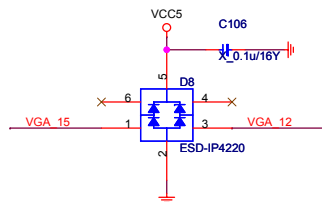
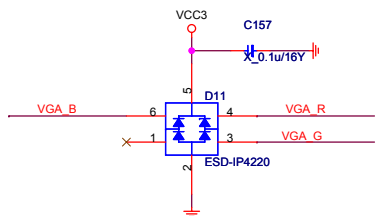
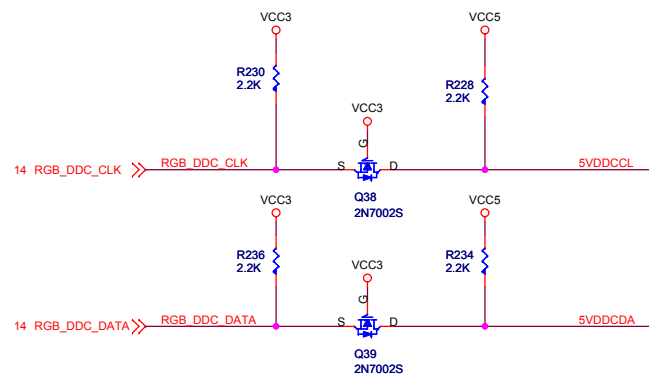
# IDE Connector



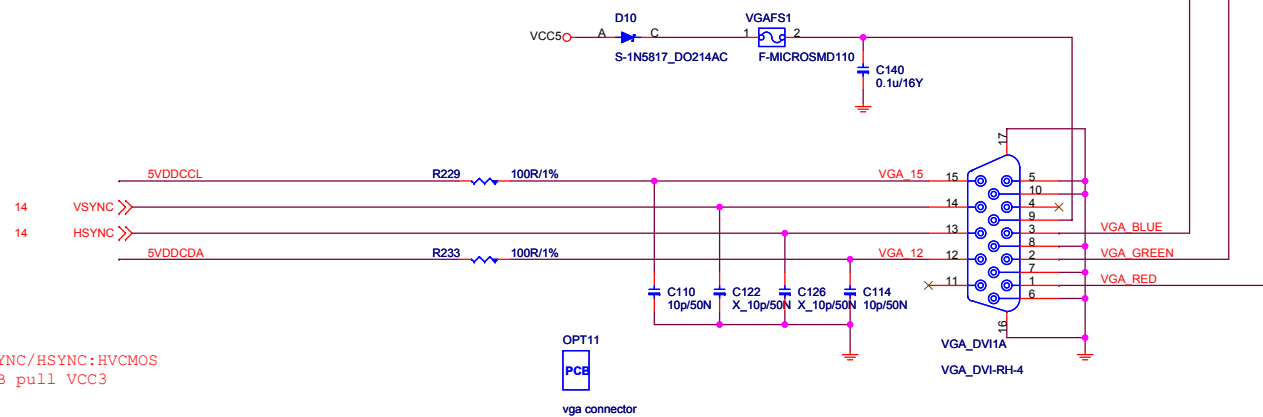
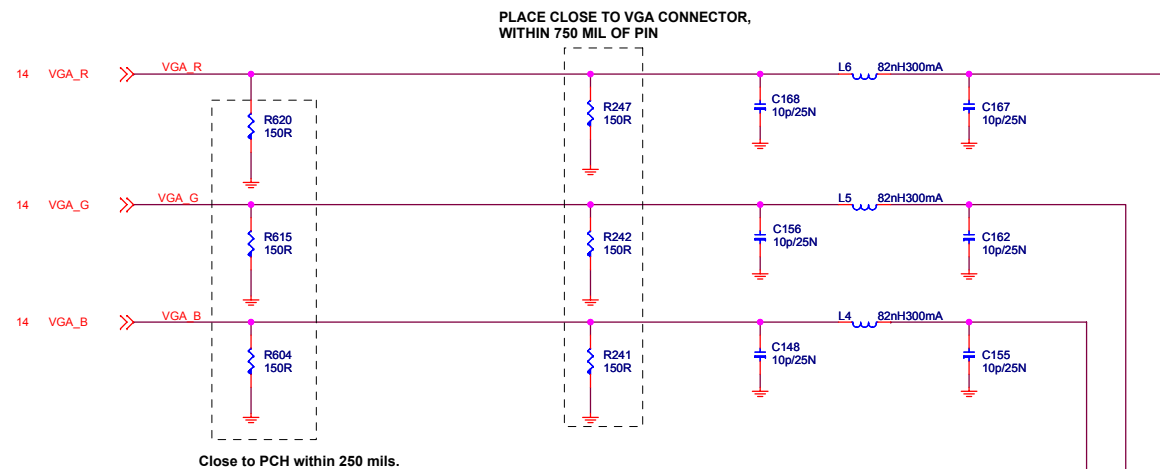
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# D-Sub

## Level shift



VSYNC/HSYNC:HVCNOS  
CRB pull VCC3

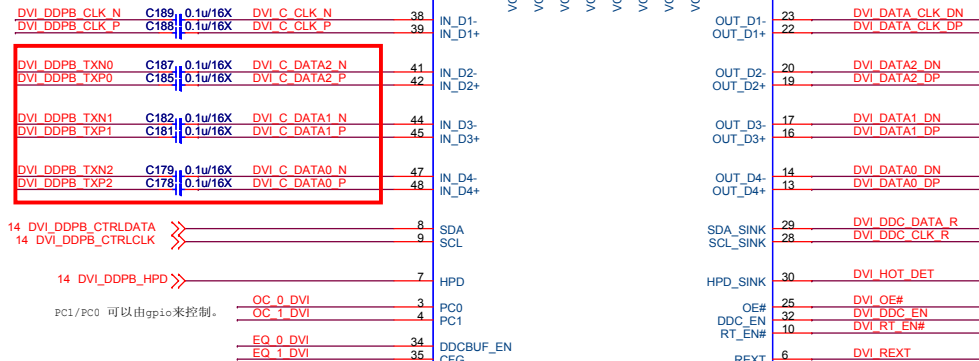


# DVI level shifter

14 DVI\_DDPB\_TXP0  
14 DVI\_DDPB\_TXN0  
14 DVI\_DDPB\_TXP1  
14 DVI\_DDPB\_TXN1  
14 DVI\_DDPB\_TXP2  
14 DVI\_DDPB\_TXN2  
14 DVI\_DDPB\_CLK\_P  
14 DVI\_DDPB\_CLK\_N

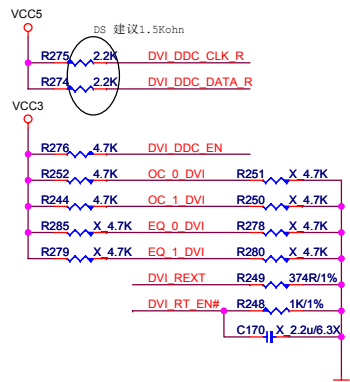
## PCH signal Mappings DG P156

差分阻抗为100ohm

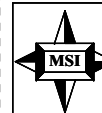
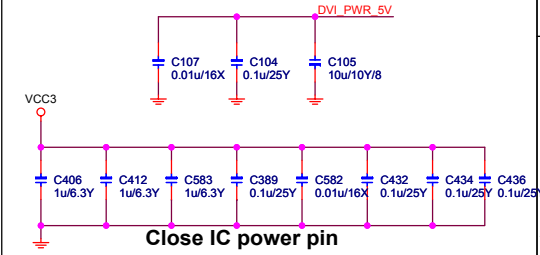
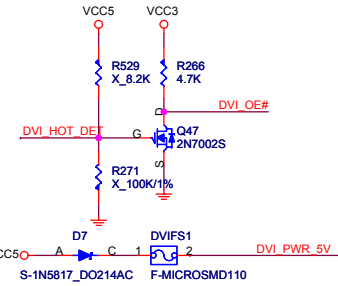
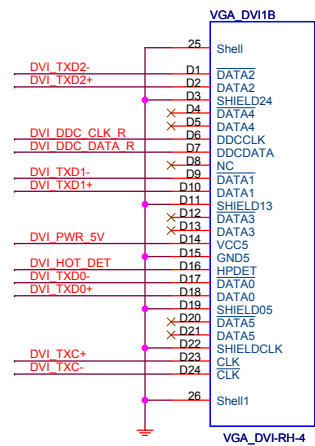
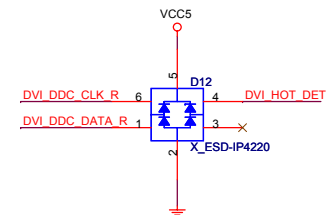


PC1/PC0 可以由gpio来控制。

PARADE 腹:B0B-081010C-P97.



reserve



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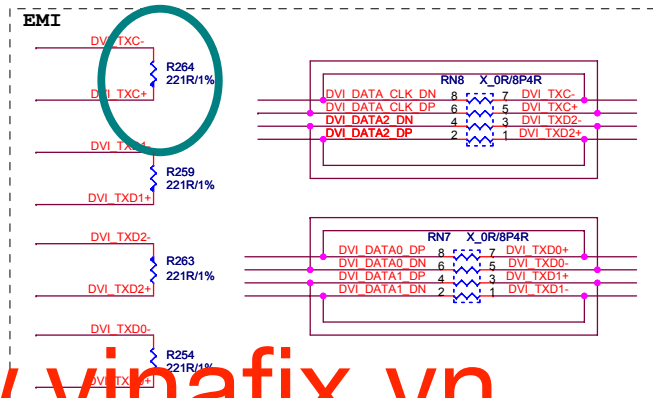
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	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

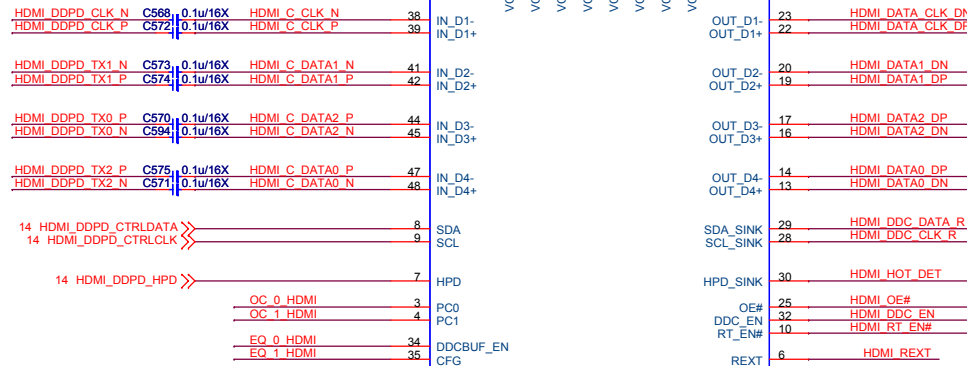
[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	The 4-dB equalization setting is recommended for PC motherboard level shifting to compensate PCB trace losses.
11	0 dB	

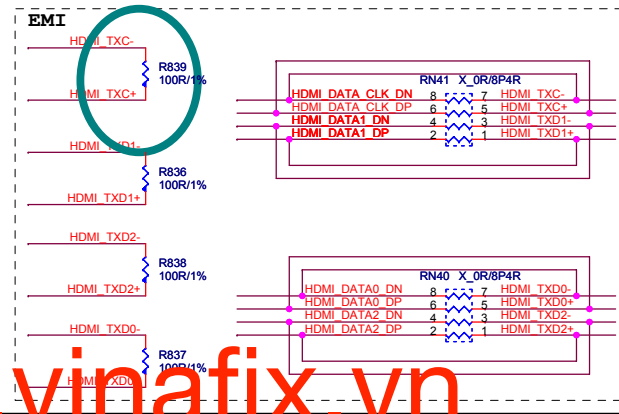
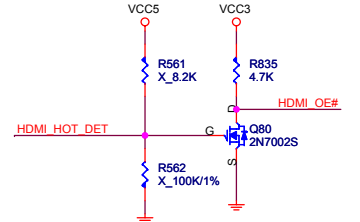
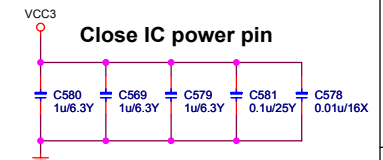
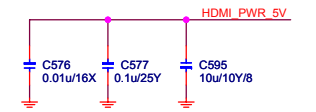
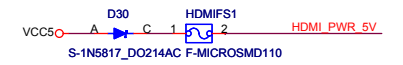
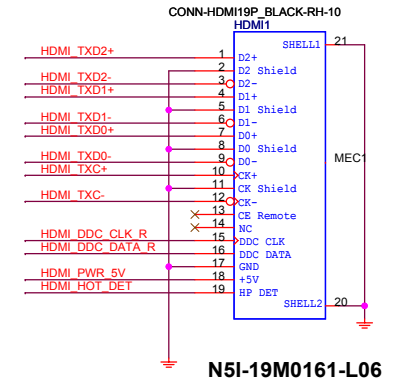
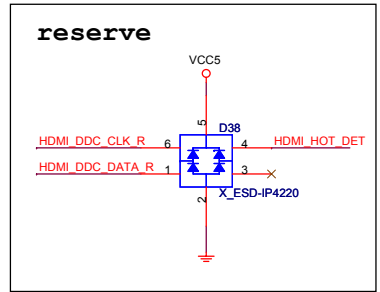


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# HDMI level shifter



PERICOM 腹:B0B-411LS2C-P22.  
PARADE 腹:B0B-081010C-P97.



	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

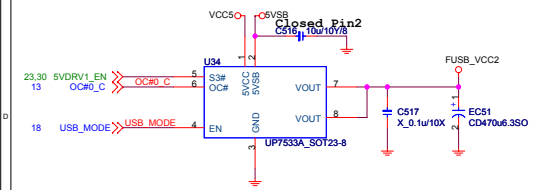
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**MS-7587**  
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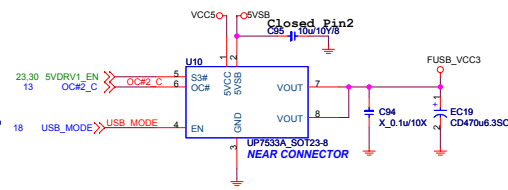


## Rear USB Connector

### USB POWER FOR PORT 0,1

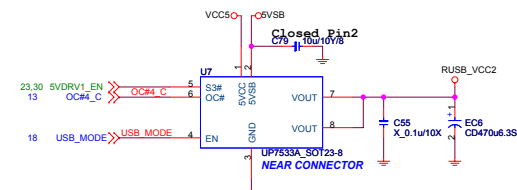


### USB POWER FOR PORT 4,5

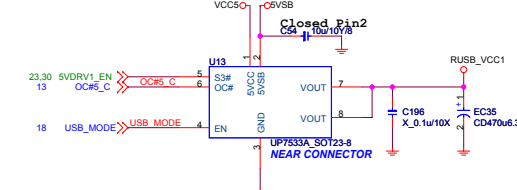


## Front USB Connector

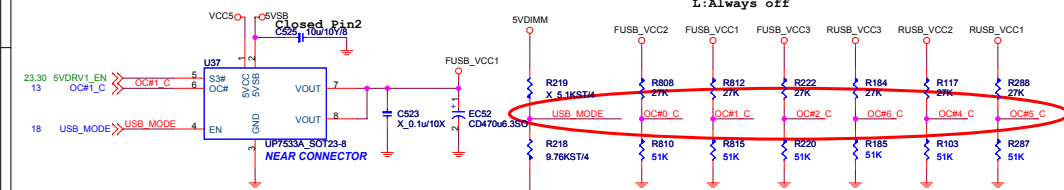
### USB POWER FOR PORT 6,7



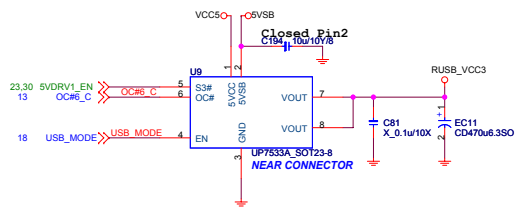
### USB POWER FOR PORT 8,9



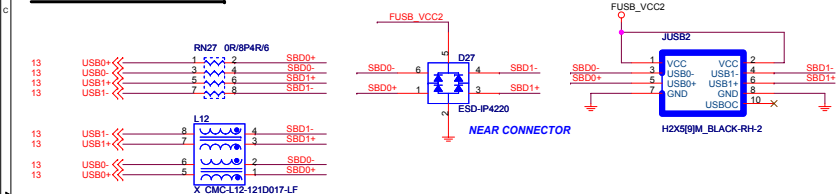
### USB POWER REAL PORT 2,3



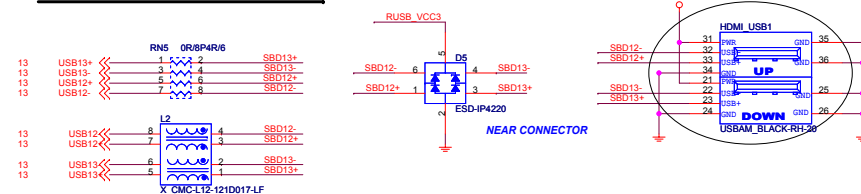
### USB POWER FOR PORT 10,11



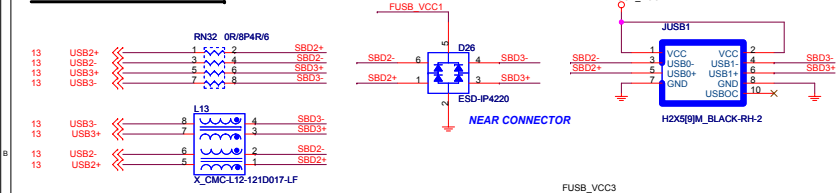
## FRONT USB PORT 0,1



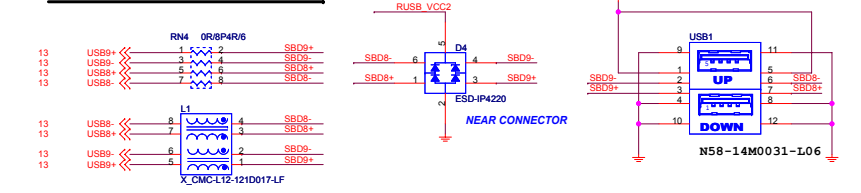
## REAR USB PORT 12,13



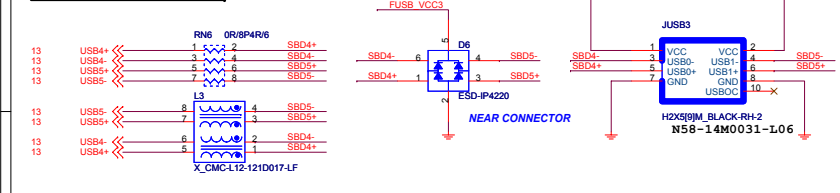
## FRONT USB PORT 2,3



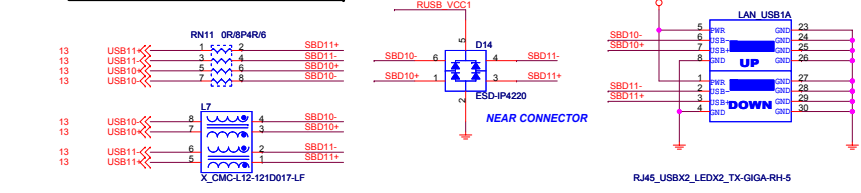
## REAR USB PORT 8,9



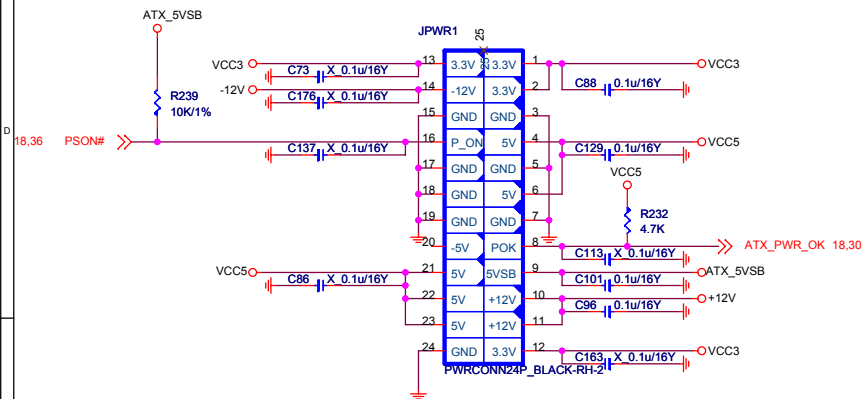
## Front USB PORT 4,5



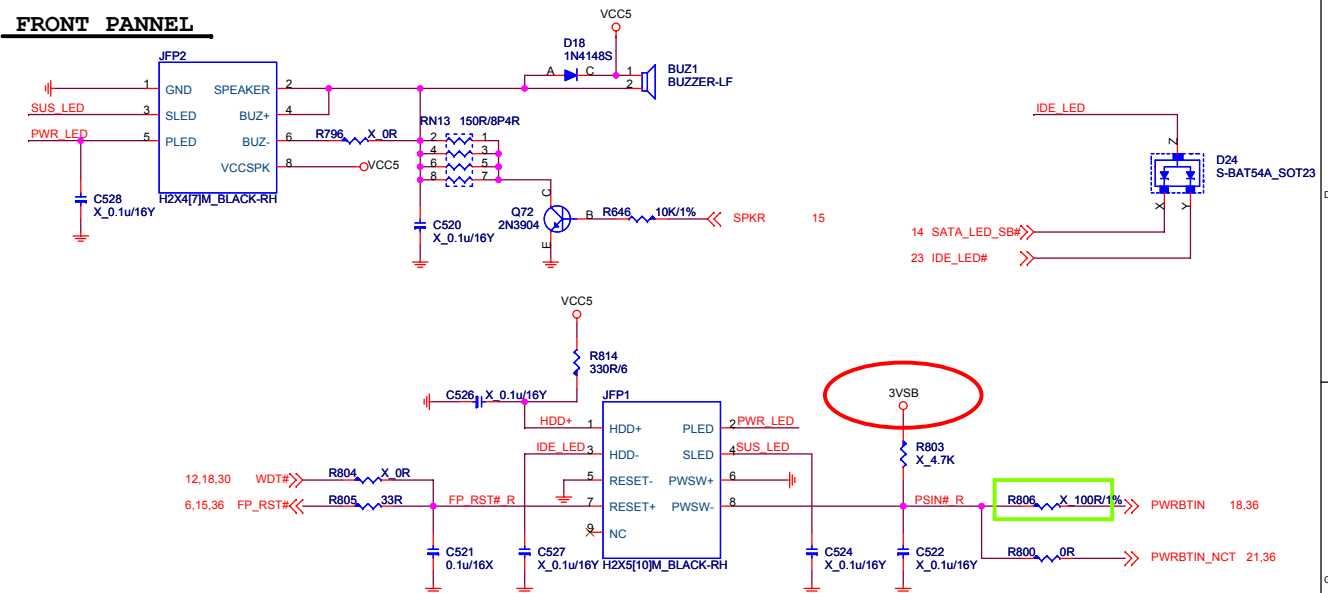
## REAR USB PORT 8,9



## ATX POWER CONNECTOR



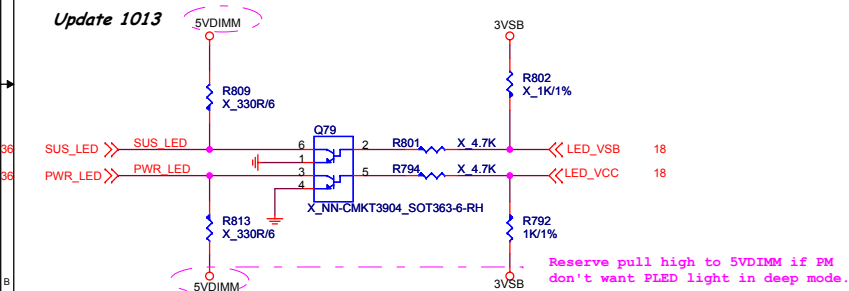
## FRONT PANNEL



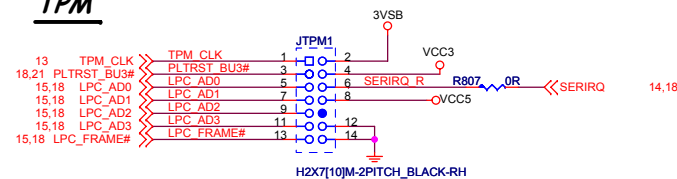
## LED ( for Fintek 71889)

If use N3016Y LED Ctrl,  
SIO LED\_VCC / LED\_VSB can not to use.

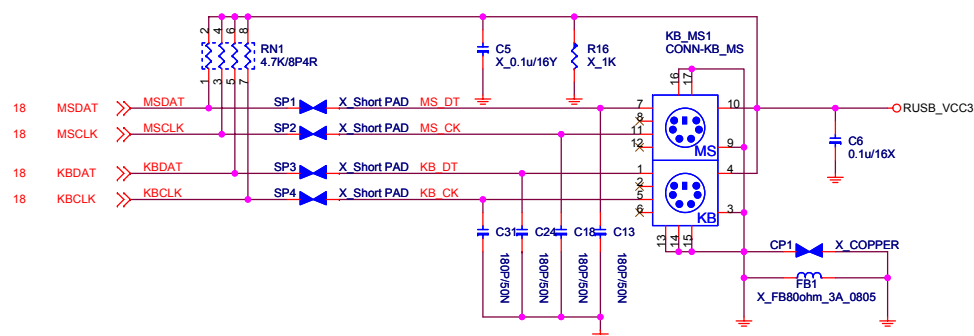
Update 1013



## TPM



## PS2 KEYBOARD & MOUSE CONNECTOR



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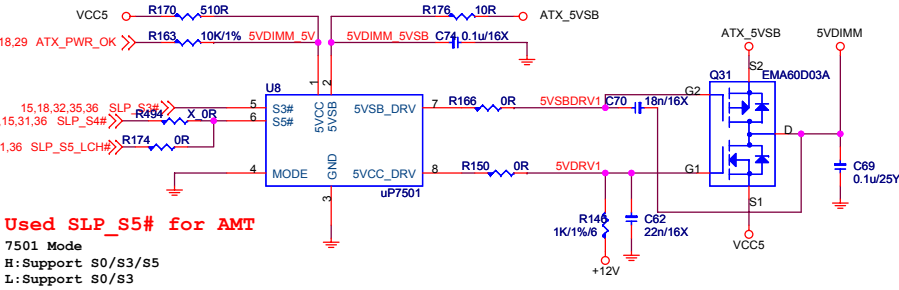


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5VDIMM FOR DDR



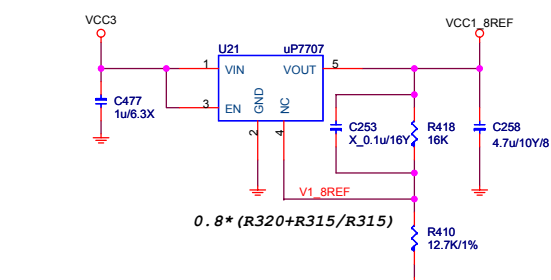
Used SLP\_S5# for AMT

7501 Mode

H:Support S0/S3/S5

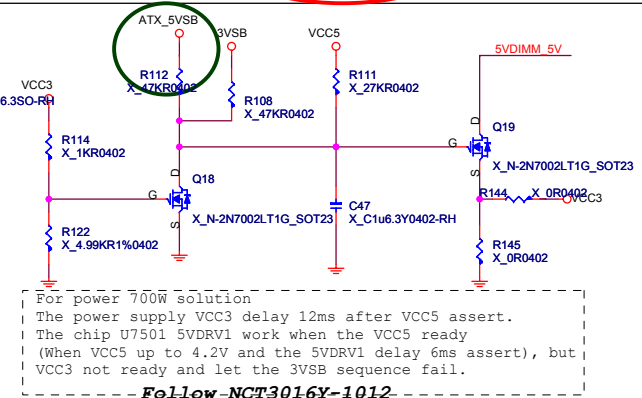
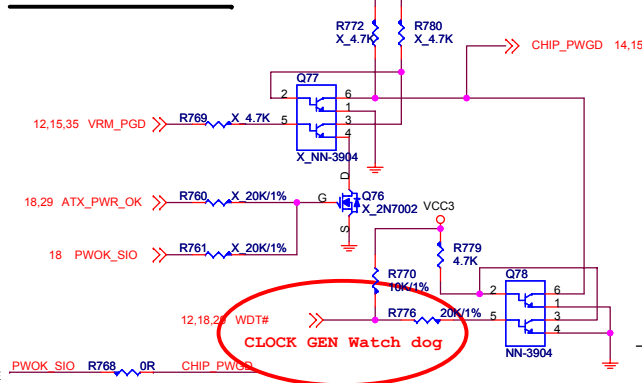
L:Support S0/S3

VCC1\_8REF



PWROK\_DELAY

VID before PWROK >3ms



For power 700W solution

The power supply VCC3 delay 12ms after VCC5 assert.

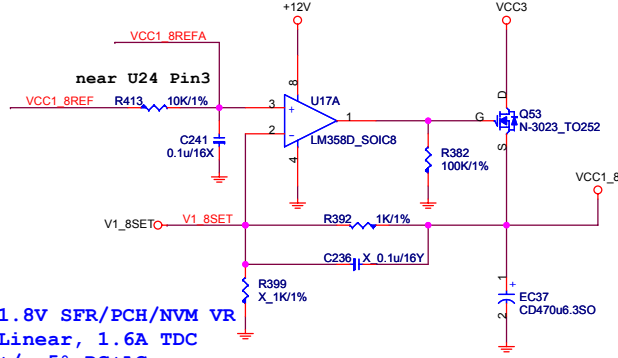
The chip U7501 5VDRV1 work when the VCC5 ready

(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but

VCC3 not ready and let the 3VSB sequence fail.

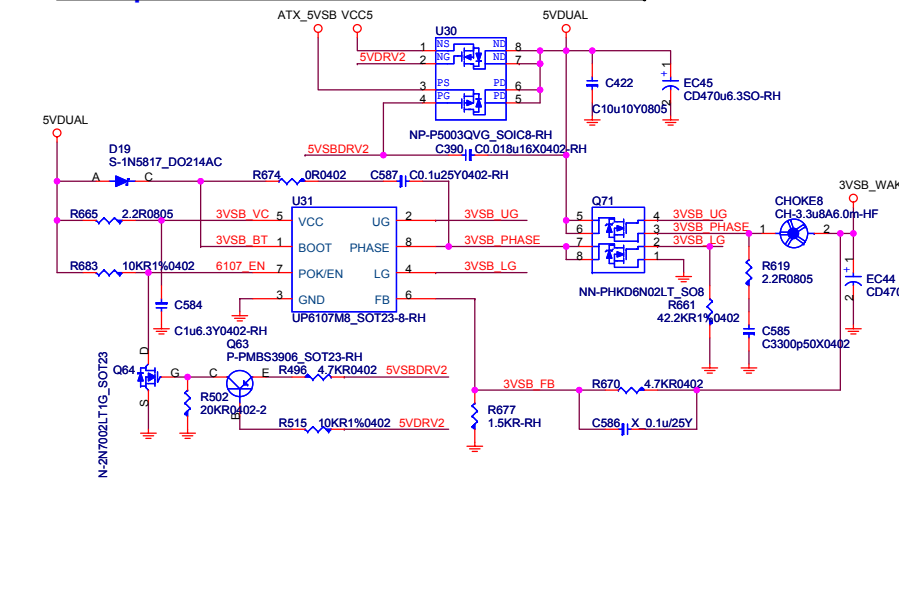
Follow NCT3016Y-1012

VCC1\_8

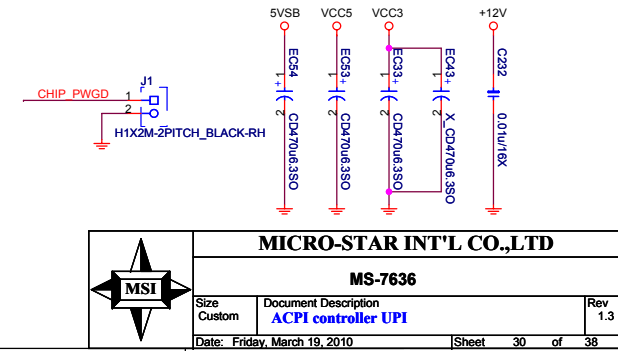
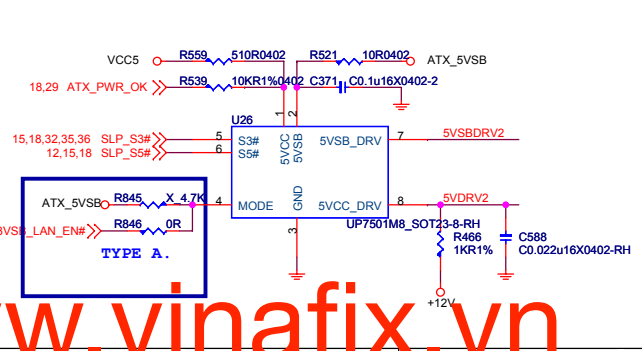
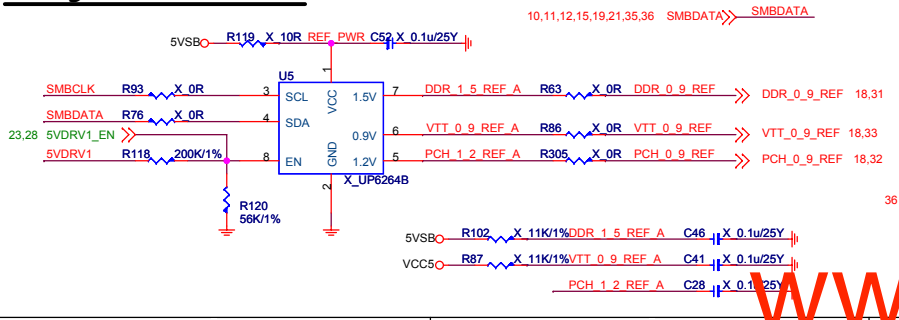


cpuvtt & pch vore wait 1.8v

Deep Mode WOL LAN Power CTRL Circuit



Voltage console

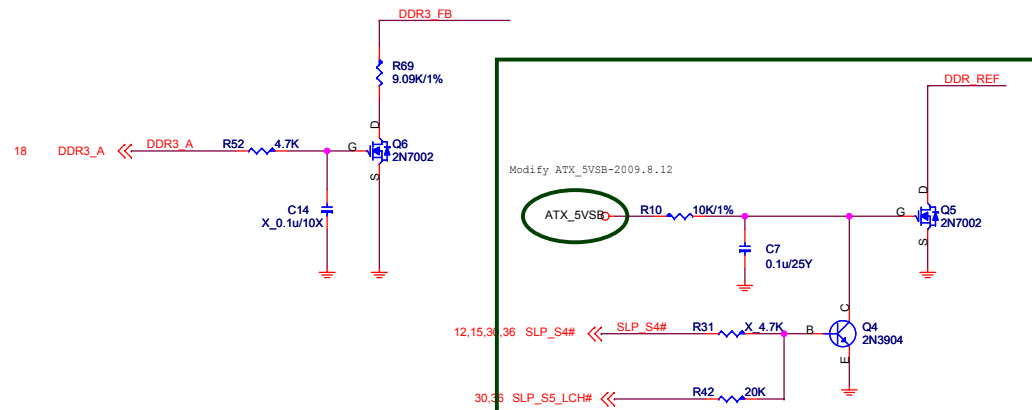
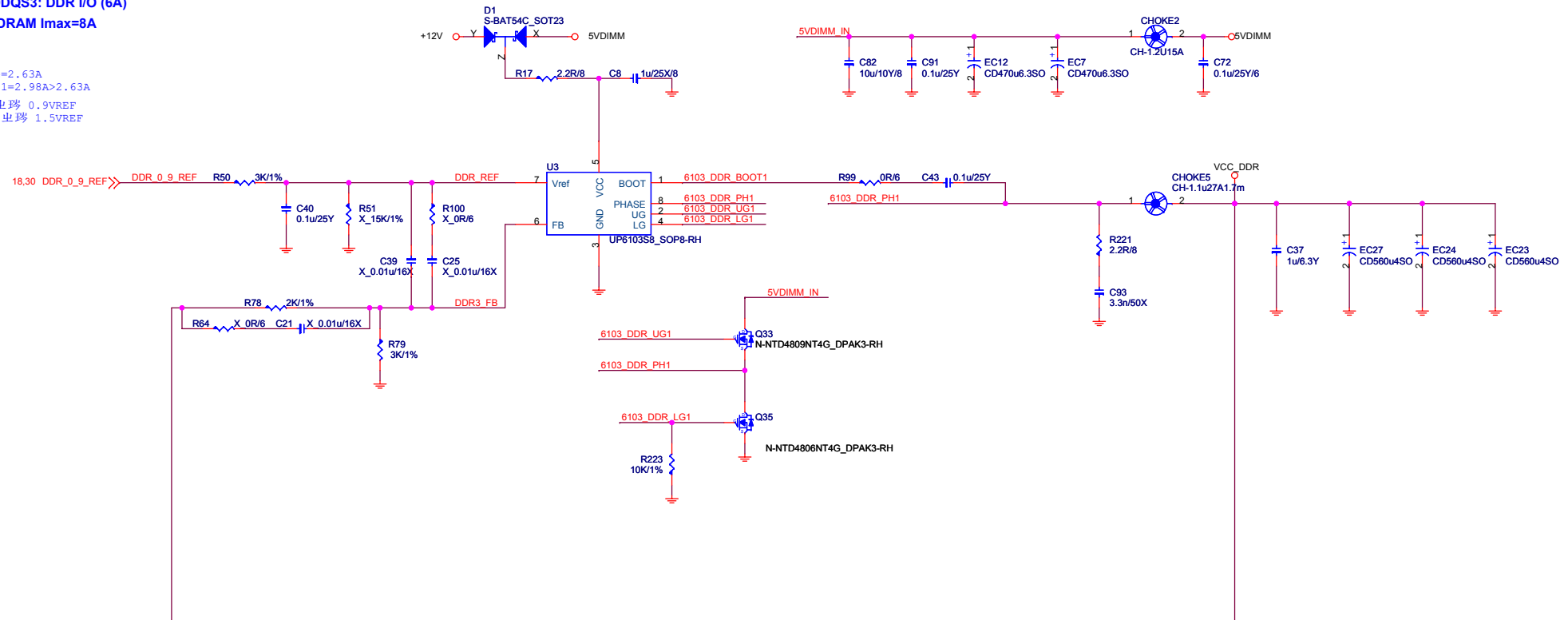


# DDR3\_1.5V

$$21.25A=6A+8A+0.75A+6.5A$$

V1.5DDQS3: DDR I/O (6A)  
DDR DRAM I<sub>max</sub>=8A

Tripple=2.63A  
1.49\*2\*1=2.98A>2.63A  
SIO 串联 0.9VREF  
6264 串联 1.5VREF

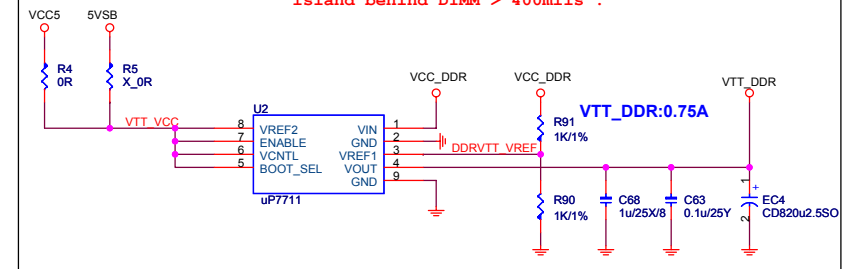


Only for meet Intel power down sequence.

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## DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



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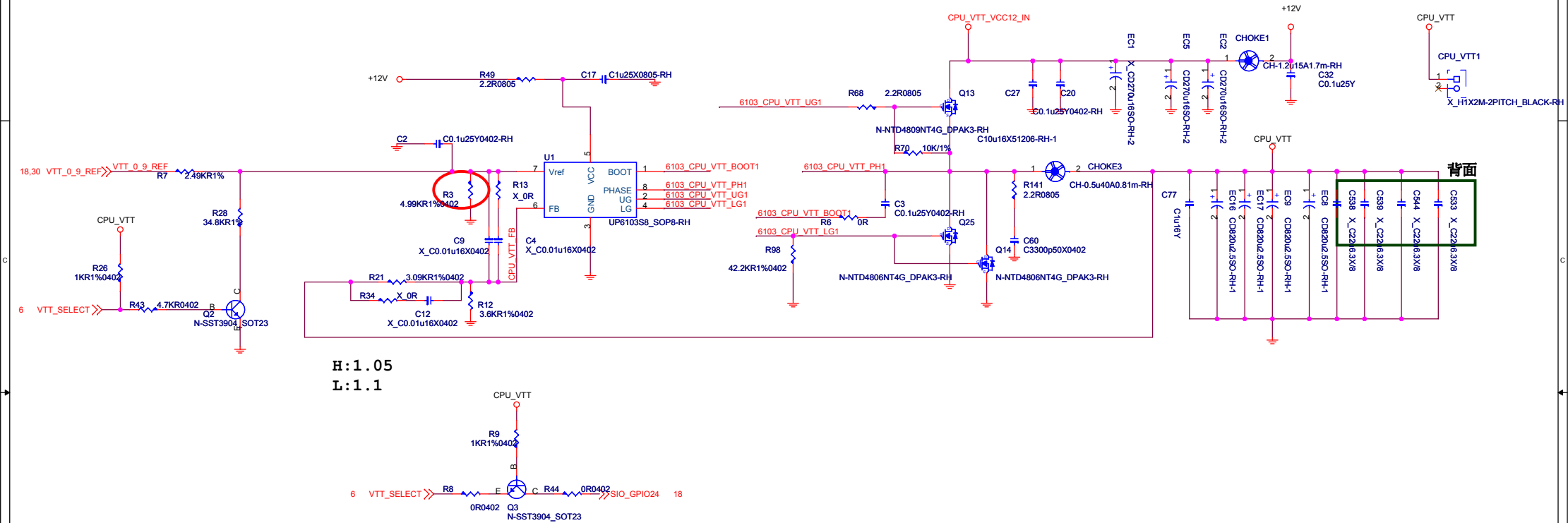


# VTPWRGD LEVEL SHIFT

## CPU\_VTT

VTT50: 1.1V/1.05V CPU Uncore, MCP I/O  
(30A)

Iripple=8.28A  
6.1\*2\*1=12.2A>8.28A



H:1.05  
L:1.1

背面



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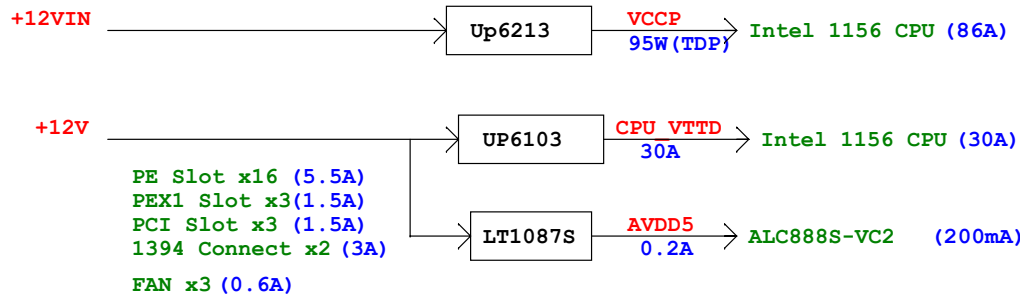
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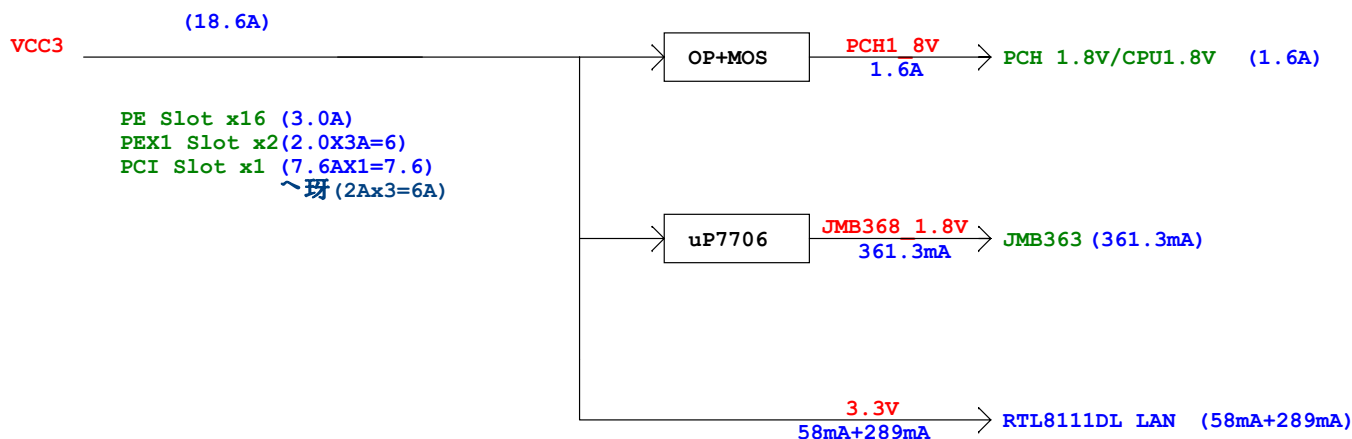
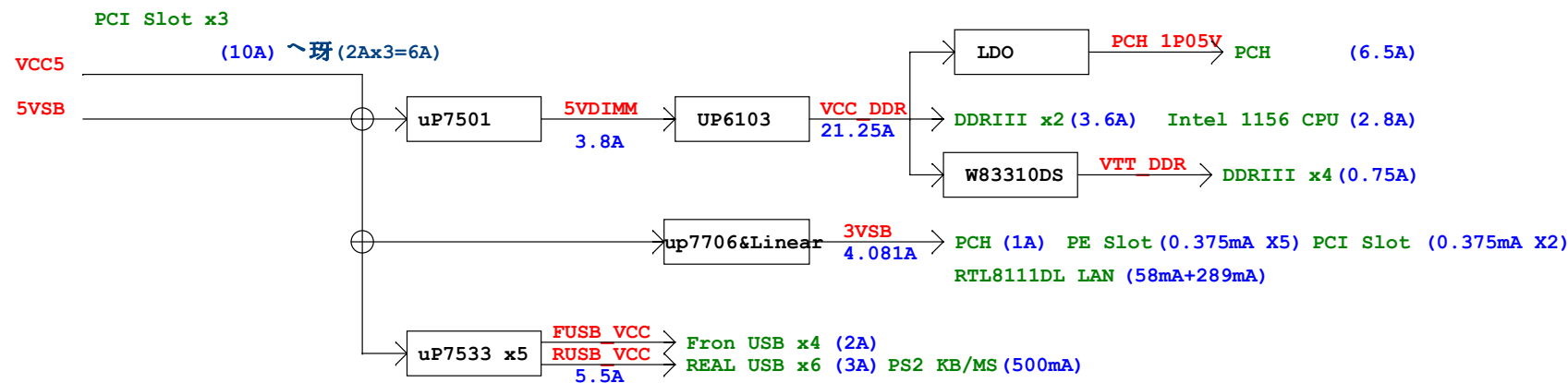
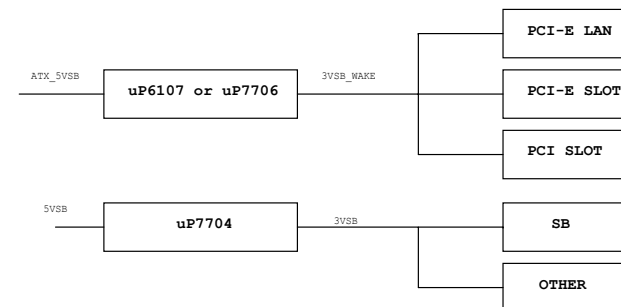




## 3VSB and 3VSB\_WAKE POWER MAP

Add- 2009.9.28

## Power Delivery



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